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Telecommunications equipment – Private Branch Exchanges (PBXs) – Attachment requirements, transmission characteristics, for digital 2048 kbit/s connection to a public switched telephone network

Telekommunikationsutrustning – Abonnentväxlar – Transmissionstekniska krav för digital 2048 kbit/s anslutning till ett allmänt tillgängligt telefonnät

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0 Introduction

This edition results from a general review of the standard SS 63 63 29 for attachment to a PSTN in order to align its mandatory content with the requirements of the teleterminal directive, 91/263/EEC, article 4(d) and some article 4(f) aspects.

Requirements for connection to leased lines and requirements for call control and signalling are covered in other Swedish or Harmonised European standards.

1 Scope

This standard covers the attachment requirements, transmission characteristics, for 2 048 kbit/s digital connection of PBXs to a public switched telephone network (PSTN) in Sweden using 120 ohms exchange line interfaces.

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2 Normative references

The following standards contain requirements which, through reference, also constitute requirements of this standard. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

ITU-T Recommendation:

G.703 Physical/electrical characteristics of hierarchical digital interfaces (1991)

ETSI documents:

TBR 4 Integrated Services Digital Network (ISDN); Attachment requirements for terminal equipment to connect to an ISDN using ISDN primary rate access (November 1995)

TBR 13 2 048 kbit/s digital structured leased lines; Attachment requirements for terminal equipment interface (January 1996)

3 Definitions and abbreviations

3.1 exchange line: A line (in this standard a 2048 kbit/s digital line or transmission link) that connects a PBX to the public switched telephone network (PSTN).

3.2 ELI: Exchange Line Interface (see figure 1).

3.3 input port: The port of the PBX at which the incoming 2048 kbit/s bit stream is received (see figure 1).

3.4 output port: The port of the PBX at which the outgoing 2048 kbit/s bit stream is transmitted (see figure 1).

3.5 holdover mode: An operating condition of a clock which has lost its controlling input and is using stored data, acquired while in locked operation, to control its output.

3.6 free running mode: An operating condition of a clock, the output signal of which is strongly influenced by the oscillating element and not controlled by servo phase-locking techniques.

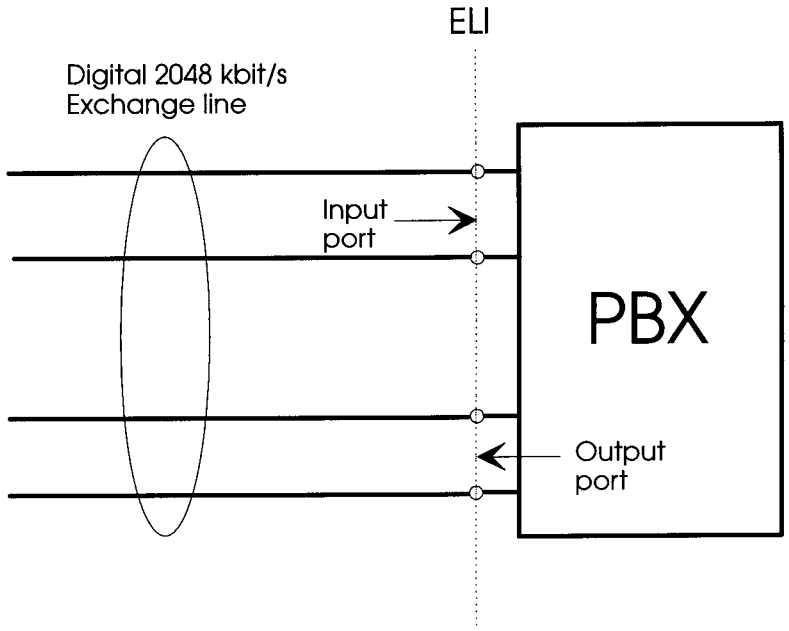

Figure 1 – Exchange line interface (ELI)

4 Requirements

4.1 General

Test methods are referred to in annex A.

4.2 Physical characteristics

4.2.1 *Hardwired connection*

The PBX shall provide

a) a set of connection contacts (e.g. an insulation displacement connector or a screw terminal block) to which solid wire conductors with diameters in the range 0,4 mm to 0,6 mm may be connected; or

b) a wiring arrangement connected by any means to the PBX, with unterminated solid wire conductors with diameters in the range 0,4 mm to 0,6 mm at the end distant from the PBX.

4.2.2 *Alternative means of connection*

Any alternative means of connection may be provided in addition to the connection arrangements under subclause 4.2.1.

NOTE – Where a wiring arrangement is provided under subclause 4.2.1 b), such a wiring arrangement need not be supplied where a means of connection which is the subject of this subclause is to be used.

4.3 Specification at output port

4.3.1 *Signal coding*

The signal transmitted at the output port shall comply with the High Density Bipolar code of order 3 (HDB3) encoding rules (see annex B).

4.3.2 *Waveform shape*

The pulse at the output port shall comply with the requirements given in table 1 and figure 2; based on ITU-T Recommendation G.703.

Table 1 – Waveform shape at output port

Pulse shape (nominally rectangular)	All marks of a valid signal shall conform with the mask (see figure 2) irrespective of the polarity. The value V corresponds to the nominal peak voltage of a mark.
Test load impedance	120 Ω non-reactive
Nominal peak voltage V of a mark	3 V
Peak voltage of a space	0 ± 0,3 V
Nominal pulse width	244 ns
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0,95 to 1,05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0,95 to 1,05

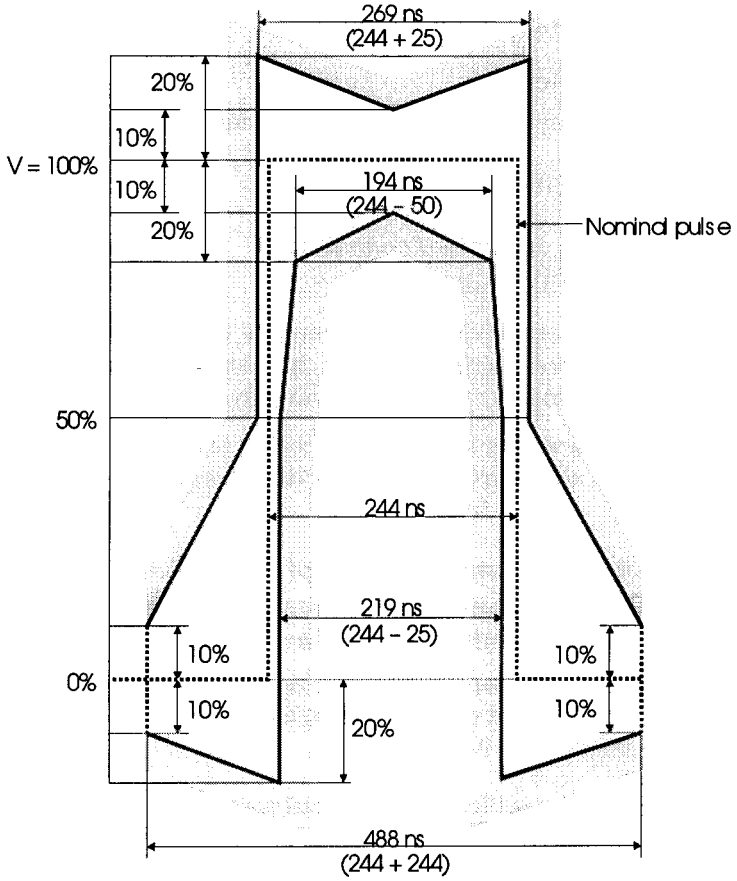

Figure 2 – Pulse mask for 2 048 kbit/s pulse

4.3.3 *Output jitter*

The peak-to-peak output jitter shall not exceed the limits of table 2 when measured with a bandpass filter having a high pass of first order (slope of 20 dB/decade) and having a low pass of third order (slope of 60 dB/decade) with cut-off frequencies as defined in the table.

For the purpose of testing, any signal input from which the output timing is derived shall be provided with the maximum tolerable input jitter, and with the maximum tolerable input frequency deviation, as specified by the manufacturer.

Where the output timing of the PBX is taken from the exchange line, the input to the PBX shall be provided with components of sinusoidal jitter in the range 1 Hz to 100 kHz at points on the curve of table 3 and figure 3.

Table 2 – Maximum output jitter

Measurement filter bandwidth		**Output jitter**
Lower cut-off (high pass)	Upper cut-off (low pass)	Unit interval (UI) peak to peak (maximum)
20 Hz	100 kHz	1,1 UI
40 Hz	100 kHz	0,11 UI

Table 3 – Input jitter for output jitter measurement

Peak-to-peak amplitude UI			**Frequency** Hz				
A_0	A_1	A_2	f_0	f_1	f_2	f_3	f_4
20,5	1,5	0,2	12×10^{-6}	20	2 400	18 000	100 000
NOTE – Although f_0 is 12 µHz, this value is only included for the purposes of correctly specifying the slope of the graph in figure 3. No requirement applies below 1 Hz.							

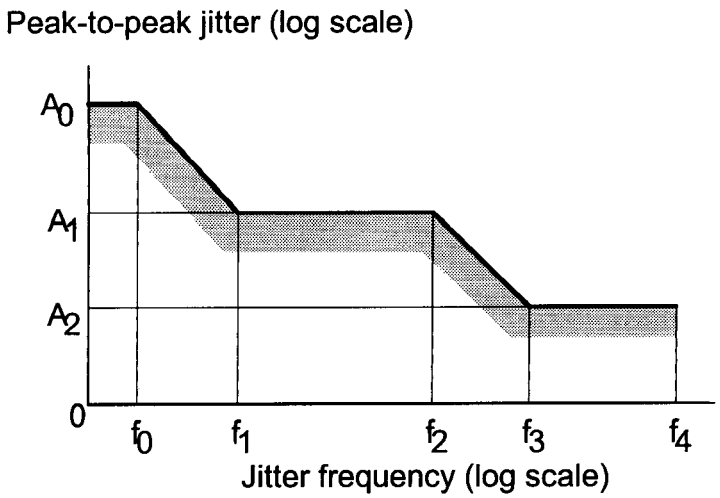

Figure 3 – Input jitter for output jitter measurement

4.3.4 *Sending power limitations, where the output signal is generated within the PBX*

4.3.4.1 *Mean power level*

The mean power level in the frequency range 300 Hz to 3 400 Hz in any one-minute period shall not be greater than -9 dBm0.

4.3.4.2 *Power level in a 10 Hz bandwidth*

The power level within a 10 Hz bandwidth centred at any frequency within the frequency range 300 Hz to 3 400 Hz, and wholly contained within that frequency range, shall not exceed -6 dBm0.

However, if the internal signal source is generating DTMF tones, the power level in a 10 Hz bandwidth between the frequencies 1 200 Hz and 1 700 Hz shall not exceed -3 dBm0.

4.3.5 *Output structure*

The bit stream transmitted at the output port of the PBX shall be structured as defined in annex C, clause C.1.

4.3.5.1 *Use of bit 1 in time slot 0*

The PBX shall comply either with a) or b) below:

a) PBXs capable of providing CRC-4: The CRC-4 bits transmitted at the output port of the PBX shall be as defined in annex C, clause C.2. However, it shall be possible to disable CRC-4 by setting bit 1 in time slot 0 transmitted at the output port of the PBX to binary ONE.

   NOTE – CRC-4 can only be applied if the network supports this feature.

b) PBXs not capable of providing CRC-4: Bit 1 in time slot 0 transmitted at the output port of the PBX shall be set to binary ONE.

4.3.5.2 *Use of the A-bit (RAI) in time slot 0*

The A-bit (RAI) transmitted at the output port of the PBX shall be set to binary ZERO except in alarm conditions (see subclause 4.6.3 and 4.6.5).

4.3.5.3 *Use of the S_a bits in time slot 0*

The S_a bits transmitted at the output port of the PBX shall be set to binary ONE.

4.4 Specification at input port

4.4.1 *Input jitter tolerance*

There are no requirements under this standard.

NOTE – The PBX should tolerate input jitter according to ITU-T Recommendation G.823 (March 1993).

4.4.2 *Input structure*

The bit stream transmitted towards the input port of the PBX will be structured as defined in annex C, clause C.1.

However, there are no requirements for time slot 0 under this standard beyond those set forth in subclauses 4.6.3-4.6.5.

4.4.2.1 *Use of bit 1 in time slot 0*

There are no requirements under this standard.

NOTE – Bit 1 in time slot 0 at the input port of the PBX is at present undefined, therefore, the PBX should be capable of accepting any value of this bit, e.g. CRC-4.

4.4.2.2 *Use of the A-bit (RAI) in time slot 0*

See subclause 4.6.4.

NOTE – The A-bit (RAI) at the input port of the PBX will be set to binary ZERO except in alarm conditions (subclause 4.6.4).

4.4.2.3 *Use of the S_a bits in time slot 0*

There are no requirements under this standard.

NOTE – The S_a bits at the input port of the PBX are undefined, therefore, the PBX should be capable of accepting any value of these bits.

4.5 Signalling structure

4.5.1 *General*

The following requirements are applicable for signalling system P7/P8 as used for channel-associated signalling via the exchange line to a public switched telephone network, implying that time slot 16 shall be used with a multiframe as set forth in section 4.5.2. This shall involve two signalling channels (bits a and b) in each direction.

NOTE – Other types of signalling systems may be used in the future.

4.5.2 *CAS multiframe*

4.5.2.1 *CAS multiframe structure*

The PBX output port shall transmit, and the PBX input port shall accept a CAS (channel associated signalling) multiframe as described below.

A CAS multiframe consists of 16 consecutive frames, numbered from 0 to 15. The multiframe alignment signal is 0000, and it occupies bits 1- 4 in time slot 16 in frame 0. See table 4.

Table 4 – CAS multiframe

Time slot 16 Frame 0	Time slot 16 Frame 1		Time slot 16 Frame 2			Time slot 16 Frame 15	
0000xyxx	abcd channel 1	abcd channel 16	abcd channel 2	abcd channel 17		abcd channel 15	abcd channel 30

NOTE 1 – Channel numbers refer to telephone channel numbers. 64 kbit/s channel time slots 1 to 15 and 17 to 31 are assigned to telephone channels numbered from 1 to 30.

NOTE 2 – This bit allocation provides four 500-bit/s signalling channels designated a,b,c and d for each channel for telephone and other services. With this arrangement, the signalling distortion of each signalling channel introduced by the digital transmission system, will not exceed ± 2 ms.

4.5.2.2 *Requirements at the output port*

Bits c and d are not used in signalling system P7/P8 and shall have the values: c = binary ZERO, d = binary ONE.

Bits x are spare bits which shall be set to binary ONE.

Bit y is used for alarm indication to the remote end. In undisturbed operation this bit shall be set to binary ZERO and in an alarm condition set to binary ONE as required in subclauses 4.6.6 and 4.6.8.

4.5.2.3 *Requirements at the input port*

The bits at the input port will be used in the same way as described in subclause 4.5.2.2.

However, there are no requirements under this standard beyond those set forth in subclauses 4.6.6-4.6.8."

4.6 Monitoring and detecting faults

4.6.1 *Frame alignment strategy*

Frame alignment shall be considered lost if three consecutive erroneous frame alignment signals are received.

Frame alignment shall be considered restored if the following signals are detected in three consecutive frames:

– frame alignment signal;

– absence of frame alignment signal, detected through bit 2 being equal to binary ONE in time slot 0 in the frame that does not contain the frame alignment word;

– frame alignment signal.

When, after frame alignment has been lost, a frame alignment signal is detected in frame n, but the aforesaid frame alignment conditions are not fulfilled in either or both frames n+1 and n+2, a new search shall be started 2 frames + 1 bit after the detection.

4.6.2 *Multiframe alignment strategy*

Multiframe alignment shall be considered lost when two consecutive erroneous multiframe alignment signals are received.

Multiframe alignment shall be considered restored as soon as correct multiframe alignment signal is received. Alternatively, multiframe alignment may be considered restored only after a correct multiframe alignment signal has been received and at least one bit is binary ONE in the immediately previous time slot 16.

4.6.3 *Loss of frame alignment in receiving direction*

If there is a frame alignment fault at the input port of the PBX, the A-bit (RAI) at the output port of the PBX shall be set to binary ONE, and the signalling bits for calls in progress shall be frozen until the fault condition has been cleared. However, the signalling bits shall be frozen for a maximum time of 30 s.

NOTE – The PBX should be blocked for outgoing calls until the fault condition has been cleared.

4.6.4 *Alarm indication in time slot 0 in receiving direction*

If the A-bit (RAI) at the input port of the PBX is equal to binary ONE, the signalling bits for calls in progress shall be frozen until the fault condition has been cleared. However, the signalling bits shall be frozen for a maximum time of 30 s.

NOTE – The PBX should be blocked for outgoing calls until the fault condition has been cleared.

4.6.5 *Alarm Indication Signal in receiving direction*

If an Alarm Indication Signal (AIS) is detected at the input port of the PBX, i.e. a signal that contains only binary ONEs except that a maximum of two bits are received as binary ZEROs in two consecutive frames (512 bits), the A-bit (RAI) at the output port of the PBX shall be set to binary ONE, and the signalling bits for calls in progress shall be frozen until the fault condition has been cleared. However, the signalling bits shall be frozen for a maximum time of 30 s.

NOTE – The PBX should be blocked for outgoing calls until the fault condition has been cleared.

4.6.6 *Multiframe alignment fault in receiving direction*

If multiframe alignment is lost at the input port of the PBX, i.e. two erroneous multiframe signals are received, bit 6 in time slot 16 in frame 0 at the output port of the PBX shall be set to binary ONE, and the signalling bits for calls in progress shall be frozen until the fault condition has been cleared. However, the signalling bits shall be frozen for a maximum time of 30 s.

NOTE – The PBX should be blocked for outgoing calls until the fault condition has been cleared.

4.6.7 *Alarm indication in time slot 16 in receiving direction*

If bit 6 in time slot 16 in frame 0 at the input port of the PBX is equal to binary ONE, the signalling bits for calls in progress shall be frozen until the fault condition has been cleared. However, the signalling bits shall be frozen for a maximum time of 30 s.

NOTE – The PBX should be blocked for outgoing calls until the fault condition has been cleared.

4.6.8 *Alarm Indication Signal in time slot 16 in receiving direction*

If an AIS is detected in time slot 16 at the input port of the PBX, i.e. a signal with all bits set to binary ONE in that time slot, bit 6 in time slot 16 in frame 0 at the output port of the PBX shall be set to binary ONE, and the signalling bits for calls in progress shall be frozen until the fault condition has been cleared. However, the signalling bits shall be frozen for a maximum time of 30 s.

NOTE – The PBX should be blocked for outgoing calls until the fault condition has been cleared.

4.7 Network synchronisation requirements and clock functions

4.7.1 *Timing*

The timing conditions shall be as follows:

- the PBX clock shall be synchronised to the incoming 2048 kbit/s signal from the exchange line (master-slave network synchronisation in which the PBX is the slave);
- the timing of the outgoing 2048 kbit/s signal shall be controlled by the PBX clock;
- if there are no acceptable synchronisation signals, the timing of the PBX shall be controlled from its own clock (holdover or free-running mode).

4.7.2 *General clock requirements*

The free-running clock frequency shall not deviate more than ± 50 ppm from the nominal value.

NOTE – It should be possible to synchronise the clock with an incoming timing signal that deviates ± 10 ppm from the nominal value.

4.8 Gain limitation

There is no requirement on the level of the output signal in the frequency range 300 to 3 400 Hz where the output signal is derived from another electrical interface by through connection. However, the gain in each transmission direction shall not, at any frequency within the range 300 to 3 400 Hz, exceed 10 dB between the ELI and any other electrical 4-wire interface, and not exceed 1 dB between the ELI and any other electrical 2-wire interface. These requirements shall be fulfilled by supplier's declaration. Furthermore, the gain in each transmission direction between two ELIs shall not exceed 0,2 dB.

NOTE 1 – It is recommended that gain is only used for compensation of line loss.

NOTE 2 – Special attention regarding stability should be given to calls where more than two interfaces are connected together within the PBX, e.g. conference calls.

4.9 Safety

There are no safety requirements under this standard.

NOTE – Safety requirements are imposed under directive 73/23/EEC, and articles 4(a) and 4(b) of directive 91/263/EEC.

4.10 EMC

There are no EMC requirements under this standard.

NOTE – There are no specific EMC requirements arising from article 4(c) in directive 91/263/EEC, and consequently all EMC aspects are covered by directive 89/336/EEC

Annex A
(normative)

Test methods

The test methods given in annex B of TBR 4 and in annex A of TBR 13 shall be applied, where applicable. For test methods not included in TBR 4 or TBR 13, it has not been deemed necessary to include details of such test methods in this standard.

Annex B
(normative)

Definition of HDB3 code

B.1 General

This annex specifies the modified Alternate Mark Inversion (AMI) code HDB3. The contents of this annex are based on annex A of ITU-T Recommendation G.703.

In this code, binary 1 bits are represented by alternate positive and negative pulses, and binary 0 bits by spaces. Exceptions are made when strings of successive 0 bits occur in the binary signal.

In the definition below, B represents an inserted pulse corresponding to the AMI rule, and V represents an AMI violation.

B.2 Definition

Each block of 4 successive binary ZEROs is replaced by 000V or B00V. The choice of 000V or B00V is made so that the number of B pulses between consecutive V pulses is odd. In other words, successive V pulses are of alternate polarity so that no DC component is introduced.

Annex C
(normative)

Definition of frame structure and CRC-4

C.1 Frame structure

The bit stream shall be structured into a frame of length 256 bits, numbered 1 to 256. The number of bits per timeslot shall be eight, numbered 1 to 8. The number of timeslots per frame shall be thirty-two, numbered 0 to 31. The frame repetition rate shall be nominally 8 000 Hz. The allocation of bits 1 to 8 (timeslot 0) within the frame shall be as shown in table C.1.

Table C.1 – Allocation of bits 1 to 8

Bit	Frame containing the frame alignment signal	Frame not containing the frame alignment signal
1	1 (see note 1)	1 (see note 1)
2	0	1
3	0	A (see note 2)
4	1	S_{a4} (see note 3)
5	1	S_{a5} (see note 3)
6	0	S_{a6} (see note 3)
7	1	S_{a7} (see note 3)
8	1	S_{a8} (see note 3)

NOTE 1 – CRC-4 may be provided (see subclause 4.3.4.1).

NOTE 2 – Bit A = Remote Alarm Indication(RAI). See subclause 4.6.

NOTE 3 – Bits S_{a4} to S_{a8} are for the use of the network operator. Their value at the output port of the PBX shall be set to binary ONE (see subclause 4.3.4.3). Their value at the input port of the PBX is undefined (see subclause 4.4.1.3).

C.2 CRC-4

C.2.1 Allocation of CRC-4 bits

The allocation of the CRC-4 bits, if provided, shall be as given in table C.2 for a complete CRC-4 multiframe. Each CRC-4 multiframe, which is composed of 16 frames numbered 0 to 15, shall be divided into two 8-frame SMFs, designated SMF I and SMF II which shall signify their respective order within the CRC-4 multiframe structure. The SMF is the block (size 2 048 bits) for the CRC-4.

In those frames containing the frame alignment signal, bit 1 shall be used to transmit the CRC-4 bits. These shall be the 4 bits designated C_1, C_2, C_3 and C_4 in each SMF. In those frames not containing the frame alignment signal, bit 1 shall be used to transmit the six bit CRC-4 multiframe alignment signal and two CRC-4 error indication bits (E-bits). The CRC-4 multiframe alignment signal shall have the form 001011.

Table C.2 – Allocation of CRC-4 bits within a CRC-4 multiframe

	SMF	Frame	Bit 1
CRC-4 multiframe	SMF I	0	C_1
		1	0
		2	C_2
		3	0
		4	C_3
		5	1
		6	C_4
		7	0
	SMF II	8	C_1
		9	1
		10	C_2
		11	1
		12	C_3
		13	E
		14	C_4
		15	E
NOTE – There is no requirement on the value of the E-bits (see subclause 4.3.4.1)			

C.2.2 CRC-4 generation

A particular CRC-4 word, located in SMF N shall be the remainder after multiplication by x^4 and then division (modulo 2) by the generator polynomial $x^4 + x + 1$, of the polynomial representation of SMF (N-1). When representing the contents of the check block as a polynomial, the first bit in the block, i.e. frame 0 bit 1 or frame 8 bit 1, shall be taken as the most significant bit. Similarly, C_1 is defined to be the most significant bit of the remainder and C_4 the least significant bit of the remainder.

The CRC-4 encoding process is described below:

- the CRC-4 bits in SMF are replaced by binary ZEROs;
- the SMF is then acted upon by the multiplication/division process defined above;
- the remainder resulting from the multiplication/division process is stored, ready for insertion into the respective CRC-4 locations of the next SMF.

NOTE – The CRC-4 bits thus generated do not affect the result of the multiplication/division process in the next SMF because, as indicated in a) above, the CRC-4 bit positions in an SMF are initially set to binary ZERO during the multiplication/division process.